Amendments to the Claims:

This listing of claims will replace all prior versions, and listings of claims in the application

Listing of Claims:

Claims 1-52 (cancelled)

Claim 53 (currently amended) In a data processing system, a method for ordering a plurality of memory access requests from a plurality of data processors, the method comprising:

accepting the plurality of memory access requests in an initial order sequence;

~~ordering the plurality of memory access requests, wherein the plurality of memory requests are ordered based on age and availability of corresponding memory locations; and~~

~~after the ordering, servicing the plurality of memory requests~~

determining whether there are available target memory addresses associated with the plurality of memory access requests;

determining whether each of the plurality of memory access requests are read requests or write requests;

determining the age of each of the plurality of memory access requests;

determining an order of precedence based on the available target memory addresses, whether the plurality of memory access requests are read requests or write requests, and the age of each of the plurality of memory access requests, wherein a first precedence is given to the memory access requests having available target memory addresses, a second precedence is given to the memory access requests that are read memory requests, and a third precedence is given to the memory access requests that are newer in age;

reordering the initial order to a new order based on the order of precedence without regard to a status of the plurality of data processors;

servicing the plurality of memory access requests; and

reordering a data exchange resulting from the plurality of memory access requests in the initial order sequence.

Claim 54 -55 (cancelled)

Claim 56 (currently amended) In a computer system, a method for processing a plurality of memory access requests from a plurality of processors, the method comprising:

receiving ~~said~~ the plurality of memory access requests ~~by a queue~~ in an initial queue;

~~reordering said plurality of memory access requests in the queue based on their age and the availability of target memory addresses, wherein a target memory address is associated with a memory access request of the plurality of memory access requests;~~

~~after said reordering, servicing said plurality of memory access requests~~

reordering the memory access requests according to a predetermined precedence order defined by a set of rules, without regard to the state of the plurality of processors, wherein the rules comprise:

establishing a first precedence for any of the plurality of memory access requests that have a corresponding available target address;

establishing a second precedence for any of the plurality of memory access requests that are read requests;

establishing a third precedence for any of the plurality of memory access requests based on age of the plurality of memory access requests; and

servicing the plurality of memory access requests.

Claim 57 (currently amended) The method of claim 56 wherein ~~said~~ the reordering provides for at least two memory access requests with available target memory addresses.

Claim 58 (currently amended) The method of claim 56 wherein ~~said~~ the servicing is done sequentially.

Claim 59 (currently amended) The method of claim 56 wherein ~~said~~ the queue is a priority queue, wherein a first memory access requests with the first precedence ~~higher priority than a second memory access request~~ is executed before ~~said~~ a second memory access request having the second precedence, and a third memory access request is processed after any of the memory requests with the first precedence or any of the memory requests with the second precedence.

Claim 60 (currently amended) The method of claim 56 wherein ~~said~~ the reordering results in a queue having a first memory access request with an available target memory address preceding a second memory access request with an unavailable target memory address.

Claim 61 (currently amended) The method of claim 56 further comprising, after ~~said~~ the servicing of said plurality of memory access requests, returning results of ~~said~~ the servicing according to a received order of said plurality of memory access requests by ~~said~~ the initial queue.

Claim 62 (currently amended) A data processing system that reorders memory access requests from a plurality of data processors, the system comprising:

a request buffer for holding a plurality of memory access requests received in a first order;

an availability determiner for determining availability of memory locations requested by said plurality of memory access requests; and

a reordering unit configured to reorder the first order of the plurality of memory access requests into a second order, without regard to a status of the plurality of the processors, ~~responsive to said availability determiner for arranging said plurality of memory access requests in a second order based on request ages and the availability of memory locations, wherein a first memory request of said plurality of memory access requests with an available memory location precedes a second memory request of said plurality of memory access requests with an unavailable memory location~~ , the second order based on a first precedence of available memory locations, a second precedence based on a type of memory request, and a third precedence based on ages of the memory access requests, the reordering unit configured to reorder, the reordering unit responsive to the availability unit to determine the first precedence; and

a collision detector configured to prevent a read memory request from occurring before a write memory request has completed.

Claim 63 (currently amended) The method of claim 62 further comprising an execution unit for executing ~~said~~ the plurality of memory access requests based on ~~said~~ the second order.

Claim 64 (currently amended) A priority queue in a computer system for determining an execution order for executing a plurality of memory access requests from a plurality of processors, the priority queue comprising:

a memory unit for storing ~~said~~ the plurality of memory access requests in a receiving order; and

an ordering module for determining ~~said~~ the execution order from ~~said~~ the receiving order, ~~said execution order is based on availability of target memory addresses associated with said plurality of memory access requests as well as an initial priority of the request, the initial priority determined by identities of memory access request sources~~

the ordering module configured to determine the availability of target memory locations, whether the memory access requests includes a read memory request or a write memory request, and the age of the requests, the ordering module configured to reorder the receiving order into the execution order wherein any memory requests with available target memory locations take precedence over any other memory requests with unavailable target memory, wherein read memory requests take precedence over any write memory request, and where older memory requests take precedence over younger memory requests, regardless of the state of the plurality of processors.

Claim 65 (currently amended) The method of claim 64 wherein ~~said~~ the plurality of memory access requests comprises at least three memory access requests.

Claim 66 (currently amended) The method of claim 64 further comprising an execution unit for executing ~~said~~ the plurality of memory access requests in ~~said~~ the execution order.

Claim 67 (currently amended) The method of claim 66 further comprising a results ordering module for returning results of ~~said~~ the execution unit according to ~~said~~ the receiving order.

Claim 68 (currently amended) In a data processing system, a method for ordering a plurality of memory access requests from a plurality of processors, the method comprising:

accepting the plurality of memory access requests;

determining an initial order~~ing~~ of the plurality of memory access requests, ~~wherein the plurality of memory requests are ordered based on an initial priority and availability of a corresponding memory location, the initial priority determined by identities of memory access request sources, and wherein a first request of the plurality of memory access requests to a first memory bank that is not currently being accessed precedes a second request of the plurality of memory access requests to a second memory bank that is currently being accessed~~

determining an order of execution precedence based on available target memory location, type of memory access requested, and an age of the memory access request;

reordering the initial order of the plurality of memory access requests with respect to the execution preference, wherein the plurality of processors are unaware of the reordering; and

after the reordering, servicing ~~the first request~~ any of the plurality of memory access requests according to the execution preference.

Claim 69 (currently amended) In a computer system, a method for processing a plurality of memory access requests from a plurality of processors, the method comprising:

receiving ~~said~~ the plurality of memory access requests;

determining any available target memory address associated with the plurality of memory access requests;

determining if any of the memory access requests are read requests or write requests;

determining the age of each of the plurality of memory access requests;

comparing the available target addresses of any read requests to the target addresses of any write requests;

reordering ~~said~~ the plurality of memory access requests without regard to the status of the plurality of processors, such that the first memory access requests for servicing are those with available target memory, the second memory access requests for servicing are read and write requests, wherein read requests follow write requests that are requesting access to an identical target address, and the third memory access requests for servicing are based on age of the memory access request; and

~~based on request age and the availability of target memory addresses, wherein a target memory address is associated with a memory access request of the plurality of memory access requests and a target memory address is available if it is located in a memory bank that is not currently being accessed~~;

after ~~said~~ the reordering, servicing said plurality of memory access requests.

Claim 70 (currently amended) The method of claim 69 wherein ~~said~~ the servicing is done sequentially.

Please add the following new claims:

Claim 71 (new) The method of claim 53 wherein the status of the plurality of data processors comprises being unaware of the reordering.

Claim 72 (new) The method of claim 53 wherein the second precedence comprises only allowing a read memory request to execute after a write request has cleared from an identical target memory address being requested for the read memory request.

Claim 73 (new) The method of claim 68 wherein determining the order of execution precedence based on available target memory location comprises giving precedence to those plurality of memory access requests that have an available target memory to access.

Claim 74 (new) The method of claim 68 wherein determining the order of execution precedence based on the type of memory access requested comprises giving precedence to those plurality of memory access requests that are read requests that do not have a write request to an identical target memory address.